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PATENT

Docket No.: 49657-700

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Tsutomu YOSHIMURA, et al.

Serial No.: 09/584,728

Group Art Unit: 2816

Filed: June 01, 2000

Examiner:

For: **DIGITAL SYNCHRONOUS CIRCUIT FOR STABLY GENERATING OUTPUT
CLOCK SYNCHRONIZED WITH INPUT DATA**



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FEB 15 2001
1C 2600 MAILROOM
USPTO WASHINGTON D.C.
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REQUEST FOR CORRECTED FILING RECEIPT

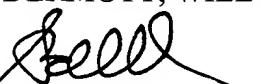
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Sir:

Attached is a copy of the Filing Receipt received from the U.S. Patent and Trademark Office in the above-referenced application. It is noted that the name of the second inventor is misspelled. Attached is a copy of the executed Declaration which contains the correct spelling of the name of the second inventor. It is requested that a corrected filing receipt be issued.

Respectfully submitted,

MCDERMOTT, WILL & EMERY


Stephen A. Becker
Registration No. 26,527

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APPLICATION NUMBER	FILING DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	DRAWINGS	TOT CLAIMS	IND CLAIMS
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09/584,728 06/01/2000 2816 690 49657-700 6 13 1

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Applicant(s)

Tsutomu Yoshimura, Hyogo, JAPAN;
Harafusa Kondoh, Hyogo, JAPAN;

HARU FUSA

Continuing Data as Claimed by Applicant

Foreign Applications

JAPAN 11-347448(P) 12/07/1999

If Required, Foreign Filing License Granted 07/26/2000

Title

Digital synchronous circuit for stably generating output clock synchronized with input data

Preliminary Class

327

Data entry by : SHIFERAW, MESERET

Team : OIPE

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